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GLITCH-FREE NAND-BASED DIGITALLY CONTROLLED DELAY LINES

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ABSTRACT

Glitch is an undesired transition that occurs before the signal settles to its intended value. It is an electrical pulse of short duration that is usually the result of a fault or design error, particularly in a digital circuit. The existing Glitch Free NAND-based Digitally Controlled Delay Lines (DCDL) presented some glitching problem which limited their applications. To overcome this limitation new NAND-based DCDL is proposed. This will maintain the same resolution and minimum delay of existing NAND-based DCDL. The proposed DCDL will be working on the basis of two control signals which are used to avoid glitches. The delay elements are composed of NAND gates. The state of the delay elements is based on the control signals. By applying control signals at minimum delay to the NAND gates, the glitches can be avoided. The driving circuits for the delay control bits are proposed.

KEYWORDS: ALL Digital circuit, glitching, DCDL.

INTRODUCTION

A glitch is a short-lived fault in a system. It is often used to describe a transient fault that corrects itself, and is therefore difficult to troubleshoot. The term is particularly common in the computing and electronics industries, and in circuit bending, as well as among players of video games, although it is applied to all types of systems including human organizations and nature. An electronics glitch is an undesired transition that occurs before the signal settles to its intended value. In other words, glitch is an electrical pulse of short duration that is usually the result of a fault or design error, particularly in a digital circuit. For example, many electronic components, such as flip-flops, are triggered by a pulse that must not be shorter than a specified minimum duration; otherwise, the component may malfunction. A pulse shorter than the specified minimum is called a glitch.

A computer glitch is the failure of a system, usually containing a computing device, to complete its functions or to perform them properly. In public declarations, glitch is used to suggest a minor fault which will soon be rectified and is therefore used as a euphemism for a bug, which is a factual statement that a programming fault is to blame for a system failure. It frequently refers to an error which is not detected at the time it occurs but shows up later in data errors or incorrect human decisions. While the fault is usually attributed to the computer hardware, this is often not the case since hardware failures rarely go undetected.

PROPOSED METHOD

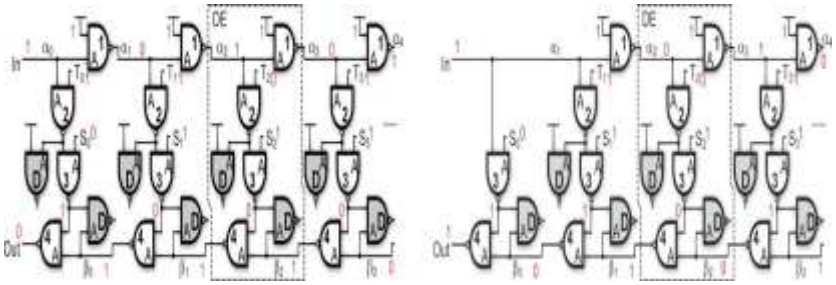


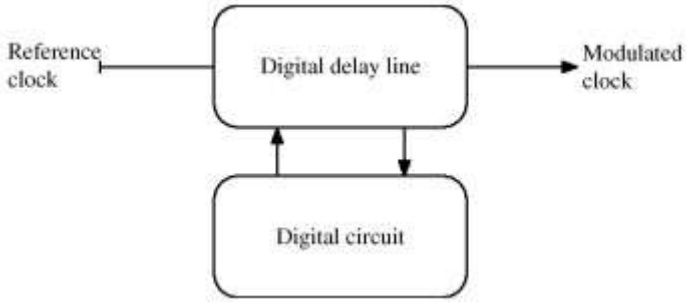
Fig 2.1 Proposed glitch-free NAND-based DCDL – inverting and non-inverting topology

The structure of proposed DCDL is shown in Fig.2.1. In this figure "A" denotes the fast input of each NAND gate. Gates marked with "D", represents dummy eells added for load balancing. Two sets of control-bits, S_i and T_i, control the DCDL. The S_i bits encode the control-code c by using thermometric code: $S_i=0$ for $i < c$ and $S_i=1$ for $i \geq c$. The bits T_i encode again c by using a one-cold code: $T_{c+1}=0$, $T_i=1$ for $i \neq c+1$. The Fig.3.3(a) shows the state of all signals in the case In=1,c=1.According to the chosen control-bits encoding, each delay-element (DE) can be in one of three possible states.

The DEs with $i < c$ are in pass-state ($S_i=0,T_i=1$) . In this state the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. The DE with i=c is in turn-state ($S_i=T_i=1$). In this state the upper input of the DE is passed to the output of NAND "3". The next DE (i=c+1) is in post-turn state ($S_i=1,T_i=0$). In this DE the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". All remaining DEs (for $i > c+1$) are again in turn-state ($S_i=T_i=1$) .

ALL DIGITAL SSCG

Fig.3.1 All digital SSCG circuit



The commonly used technique to produce SSCG is an "all analog" one where modulation is applied or inserted into a phased-lock loop (PLL). The frequency can be modulated by imposing a signal on the voltage control node of a VCO in a PLLas shown in fig. 3.1 . The technique here uses strictly only digital circuits and does not use a PLL. The circuit has an area of 0.06 mm,is fabricated in 0.15 m CMOS process and consumes 7.1 mW for the application of a 27-MHz reference clock. It is based on a digital delay line (DDLi) with a small digital circuit to control it. The DDLi is used to modulate an input clock. The electrical length of the DDLi is limited to one period of the input clock.

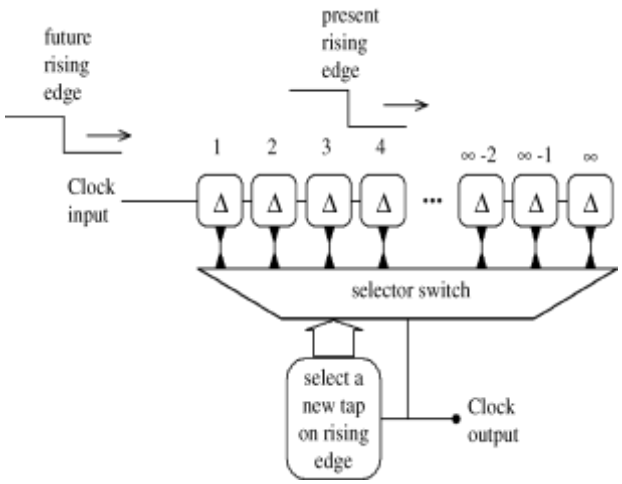


Fig.3.2 Modulating a clock with long digital delay line

Four simple concepts are outlined to understand the circuit. One can modulate the frequency of a reference clock with only a DDLi. Fig.3.2 shows such a simple setup. Let us imagine here that a new tap is selected each time a rising edge comes out. If this new tap is further down the DDLi for each rising edge, the output frequency will come down as a function of the step size for the new taps. If the step size is selected properly, one could modulate the reference clock with a triangular wave for example. The problem with this circuit is that the DDLi must be very long or infinitely long. This brings to next concept.

DIGITAL DELAY LINE (DDLI)

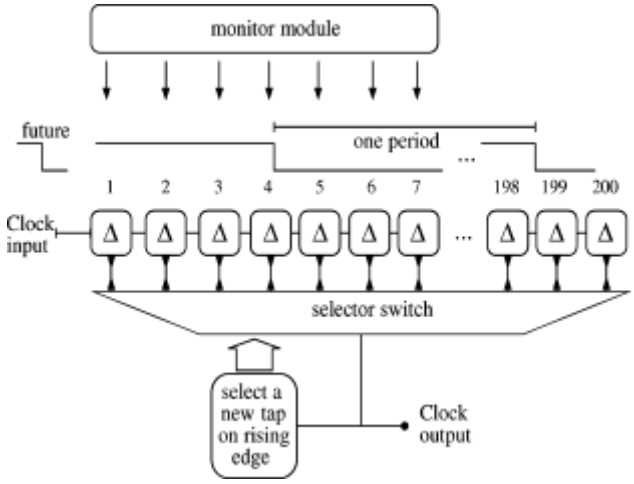


Fig 4.1 Digital delay line of finite length

Fig.4.1 shows the same circuit with a new module. The same technique is used to modulate the frequency but this time we limit the electrical length of the DDLi to a little more than one period of the reference. In that case, when the selected tap is close to the end of the DDLi, the future or next rising edge is already in the DDLi and can be seen by the monitoring module. At the time where two rising edges are present in the DDLi, one could select a new tap based on the required new tap for the correct modulation but also subtract the number of taps required for one period and come back at the beginning of the DDLi. We can now modulate down the reference clock with a simple digital delay line and dedicated digital circuit.

RESULTS AND DISCUSSION

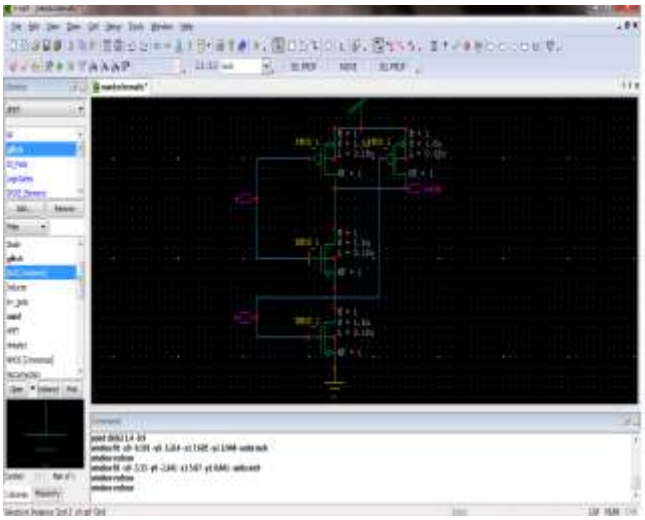


Fig 5.1 NAND gate

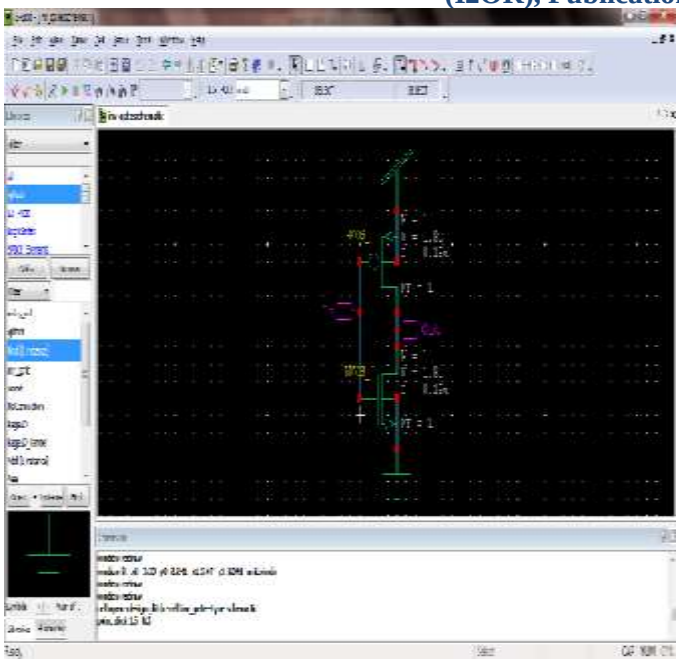


Fig 5.2 Inverter

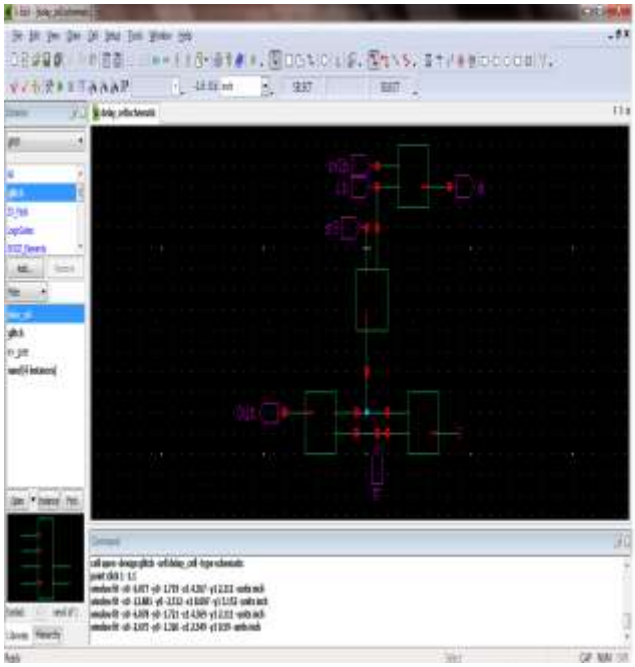


Fig 5.3 Delay element

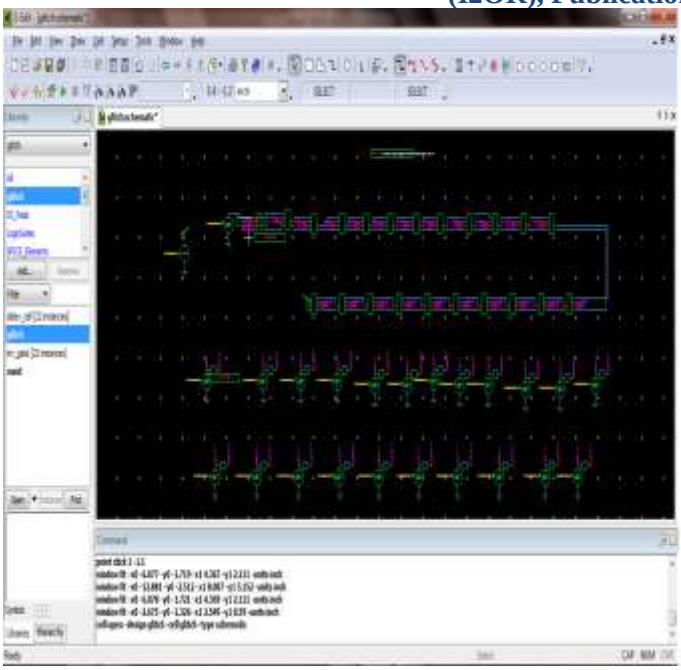


Fig 5.4 Schematic diagram of existing method

OUTPUT WAVEFORM

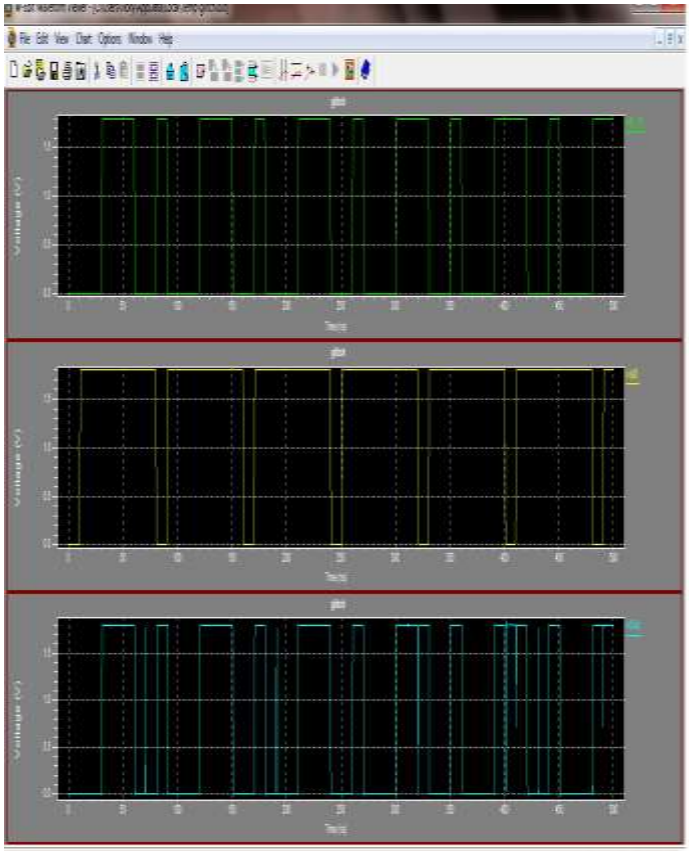


Fig 5.5 Output waveform with glitches

CONCLUSION AND FUTURE WORK

A NAND-based DCDL which avoids the glitching problem is presented. A timing model of the novel DCDL structure has been developed to demonstrate the glitch-free property of the proposed circuit. As an additional result, the developed model provides also the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation.

The simulation results has glitches and to avoid glitches proposed solution will improve the resolution with respect to previous approaches. As example application proposed DCDL is used to realize an all-digital SSCG. The employ of proposed DCDL in this circuit allowed to reduce the peak-to-peak absolute output jitter of more than the 40% with respect to an SSCG using three-state inverter-based DCDLs.

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